REMARKS

In recognition of the statements of the Examiner and in order to bring this application to allowance quickly, claims were drastically amended.

It is noted that although applicants have amended the original claims. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

The following remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

DETAILED ACTION

Double Patenting

> *3. Claims 1-20 of this application conflict with claims 1-20 of Application No. 10/619,988. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.*

In response, the applicants respectfully state that it is planned that once allowable subject matter will be defined a clear line of demarcation will be maintained between the applications.

Claim Rejections 35 USC § 102

> *4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless — (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

5. Claims 1-21 are rejected under U.S.C. 102(b) as being anticipated by Osborne et al. [US 5,751,951].

In response, the applicant respectfully states that Claims 1 - 20 are apparently not anticipated by the invention of Osborne et al. The present invention, claimed in Claims 1 - 20:

> "Methods, apparatus and systems are provided for controlling flow of data between a memory of a host computer system and a data communications interface for communicating data between the host computer system and a data communications network. In an example embodiment, apparatus comprises a descriptor table for storing a plurality of descriptors for access by the host computer system and data communications interface. Descriptor logic generates the descriptors for storage in the descriptor table. The descriptors include a branch descriptor comprising a link to another descriptor in the table."

Whereas, the cited art to Osborne et al , US Patent 5,751,951, filed: October 30, 1995, is entitled: "Network interface". The Osborne abstract reads:

> "A packet based data transmission system includes a flexible optimized non-blocking transmit interface that incorporates optimized buffer modes, dynamic and static chaining, streaming and the utilization of small packet formats. Static chaining refers to connecting together the linked list for successive packets for the same transmit channel or virtual channel. Dynamic chaining refers to means by which the network interface performs this chaining automatically, thereby solving a blocking problem. On the transmit side, streaming refers to initiating the transmission of packet data before the entire packet data has been presented to the interface. This, in turn, permits more rapid recycling of the buffer space. On the receive side, streaming refers to initiating the processing of packet data before the entire packet has been received. The packet transmission system also includes a receive interface that incorporates a chunking system in which a buffer is divided into multiple chunks or segments to accommodate different size packets. Additionally, the receive interface includes an optimized linked list scheme to support chunking in which no linking element is required for the first buffer in the linked list. In

one embodiment a small packet format is provided to reduce the relative overhead in sending small packets. In another embodiment the optimized buffer mode associated with the receive side can be utilized on the transmit interface for further reducing overhead."

Thus Osborne is concerned with a "non-blocking transmit interface that incorporates optimized buffer modes, dynamic and static chaining, streaming and the utilization of small packet formats." Osborne is not concerned with a descriptor table, or apparatus for controlling flow of data between first and second data processing systems via a memory, as in the present claims. Thus Claims 1-21 are allowable under U.S.C. 102(b) as not being anticipated by Osborne. However, claims were amended to bring this application to allowance quickly.

As for claim 1, Osborne et al teach art apparatus comprising: a descriptor table [e.g., "ring queue" in col. 1, line 59- col. 2. line 10; col. 5, lines 53-64; col. 14, lines 21- 35], said apparatus for controlling [col. 14, lines 20-35] flow of data between first [host in fig. 3A and relevant description] and second data processing systems [network interface card in fig, 3A and relevant description] via a memory, said descriptor table far storing a plurality of descriptors for access [col. 1, lines 59-64; col. 2, lines 15-21; col. 16, lines 6- 24] by the first and second data processing systems; and descriptor logic for generating [inserting into the queue using formats shown in figs, 3B-14 and relevant description; col. 2, lines 15-17; col. 15, lines 1-7; col. 19, lines 46-47) the descriptors for storage in the descriptor table the descriptors including a branch descriptor comprising a link [e.g., fig. 2A, 2B and relevant description] to another descriptor in the table.

In response, the applicants respectfully state that claim 1 is amended to clearly be novel over Osbourne. Claim 1 as amended [with emphasis shown] now reads:

1. An apparatus comprising:

a descriptor table - said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor table for storing a plurality of descriptors for access by the first and second data processing systems, said first processing system comprises a plurality of host computer systems, said second data processing comprising a plurality of attached devices interconnected by an intervening network architecture, said network architecture comprises a plurality of data communications switches, said host computer system and the attached devices each forming a node in a

data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture;

a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture; and

descriptor logic for generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

It is apparent that Osborne does not teach and does not anticipate a "first processing system comprises a plurality of host computer systems," and a "second data processing comprising a plurality of attached devices interconnected by an intervening network architecture," wherein the "network architecture comprises a plurality of data communications switches," and wherein the "host computer system and the attached devices each forming a node in a data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture." Osborne does not teach and does not anticipate "a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture." Thus claim 1 and all claims that depend on claim 1 are allowable over the cited art.

6. As for claim 2, Osborne et al teach the descriptors generated by the descriptor logic comprising a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory e.g., figs. 2A-14 and relevant description; col. 5, lines 53-64].

In response, the applicants respectfully state that claim 2 is amended to clearly be novel over Osbourne. Claim 2 as amended [with emphasis shown] now reads:

2. An apparatus as claimed in claim 1, wherein:

the network adapter comprises a pluggable option card having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system, said option card carrying:

an Integrated System on a Chip connected to the bus architecture via a connector,

at least one third level memory modules connected to the chip, and

an interposer connected to the chip for communicating data between media of the network architecture and the chip, said interposer providing a physical connection to the network, and,

wherein the descriptors generated by the descriptor logic comprise a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory.

It is apparent that Osborne does not teach and does not anticipate a "network adapter comprises a pluggable option card having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system. Osborne does not teach and does not anticipate a "option card carrying: an Integrated System on a Chip connected to the bus architecture via a connector, at least one third level memory modules connected to the chip, and an interposer connected to the chip for communicating data between media of the network architecture and the chip, said interposer providing a physical connection to the network." Thus claim 2 is allowable because of itself and because it depends on allowable claim 1.

7. As for claim 3, Osborne et at teach the descriptor table is stored in the memory of the first data processing system [host memory in col. 14, lines 32-35].

In response, the applicants respectfully state that claim 3 is amended to clearly be novel over Osbourne. Claim 3 as amended [with emphasis shown] now reads:

3. An apparatus as claimed in claim 2, wherein the memory is implemented by a combination of SRAM and SDRAM, said chip including a memory subsystem of the adapter comprises a first and a second memory, a data cache and an instruction cache associated with a TX processor, and a second data cache and second instruction cache associated with an RX processor, said three levels of memory having respective sizes and associated access times, such that the memory subsystem facilitates: convenient access to instruction and data by both the TX processor and the RX processor; scaleability; and sharing of resources between the TX processor and the RX processor in the interests of reducing manufacturing costs, and

wherein the descriptor table is stored in the memory of the first data processing system;

It is apparent that Osborne does not teach and does not anticipate an apparatus "wherein the memory is implemented by a combination of SRAM and SDRAM," wherein the "chip including a memory subsystem of the adapter comprises a first and a second memory, a data cache and an instruction cache associated with a TX processor, and a second data cache and second instruction cache associated with an RX processor." Osborne does not teach and does not anticipate "three levels of memory having respective sizes and associated access times, such that the memory subsystem facilitates: convenient access to instruction and data by both the TX processor and the RX processor; scaleability; and sharing of resources between the TX processor and the RX processor in the interests of reducing manufacturing costs. Thus claim 3 is allowable because of itself and because it depends on an allowable claim.

8. As for claim 4, Osborne et al teach the descriptor table is stored in the memory of the second data processing system [local memory of network interface card in col. 14, lines 32-35 col. 14, lines 57-58).

In response, the applicants respectfully state that claim 4 is amended to clearly be novel over Osbourne. Claim 4 as amended [with emphasis shown] now reads:

4. (Currently amended) An apparatus as claimed in ~~claim 1~~ claim 3, further permitting coexistence of heterogeneous communication protocols between the adapters and the host systems serving various applications, such that use the adapter and a predefined set of data

structures enhancing data transfers between the host and the adapter, and opening a number of application channels that can be opened in parallel as-determined by an amount of memory resources allocated to the adapter and being independent of processing power embedded in the adapter, and

wherein the descriptor table is stored in a memory of the second data processing system.

It is apparent that Osborne does not teach and does not anticipate an apparatus "permitting coexistence of heterogeneous communication protocols between the adapters and the host systems serving various applications, such that use the adapter and a predefined set of data structures enhancing data transfers between the host and the adapter, and opening a number of application channels that can be opened in parallel as-determined by an amount of memory resources allocated to the adapter and being independent of processing power embedded in the adapter." Thus claim 4 is allowable because of itself and because it depends on an allowable claim.

9. As for claim 5, Osborne et al teach the descriptor table comprising a plurality of descriptors lists sequentially inked together via branch descriptors therein [e.g., figs. 2A - 2C and relevant description].

In response, the applicants respectfully state that claim 1 is amended to clearly be novel over Osbourne. Claim 1 as amended [with emphasis shown] now reads:

5. (Currently amended) An apparatus as claimed in ~~claim 1~~ claim 3,

wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors,

wherein information in the descriptors is used for control by software in the host of data movement operations performed by TX and RX LCP engines, said information being used to process a frame to generate a TX packet header located in the header of the frame, and

wherein the descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein.

It is apparent that Osborne does not teach and does not anticipate an apparatus "wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors." Osborne does not teach and does not anticipate an apparatus, "wherein information in the descriptors is used for control by software in the host of data movement operations performed by TX and RX LCP engines, said information being used to process a frame to generate a TX packet header located in the header of the frame." Thus claim 5 is allowable because of itself and because it depends on an allowable claim.

10. As for claim 6, Osborne at al teach the descriptor table comprising a cyclic descriptor list [col. 1, lines 61-64].

11. As for claim 7, Osborne et al teach the first data processing system comprising a host computer system [host in fig. 3A and relevant description].

12. As for claim 8, Osborne et al teach the second data processing system comprising a data communications interface for communicating data between a host computer system and a data communications network [host and network interface card in fig. 3A and relevant description).

13. As for claim 9, Osborne et al teach a host computer system having a memory, a data communications interface for communicating data between the host computer system and a data communications network for controlling flow of data between the memory of the host compute; system and the data communications interface [fig. 3A and relevant description].

In response, the applicants respectfully state that claims 6-9 are each allowable at least because each depends on allowable claim 1.

14. As for claim 10, Osborne et al teach a method comprising controlling flow of data between first and second data processing systems via a memory, the steps of controlling comprising storing [e.g., figs. 2A - 2C and relevant description) in a descriptor table a plurality of descriptors for access [col. 3, lines 28-42] by the first and second data processing systems; and by descriptor logic, generating [e.g., col. 19, lines 46-47) the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link [e.g., fig. 2A and relevant description] to another descriptor in the table.

In response, the applicants respectfully state that claim 10 is amended to clearly be novel over Osbourne. Claim 10 as amended [with emphasis shown] now reads:

10. A method comprising:

controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising: storing in a descriptor table a plurality of descriptors for access by the first and second data processing systems,

forming said first processing system to comprise a plurality of host computer systems, said second data processing to comprise a plurality of attached devices interconnected by an intervening network architecture, said network architecture comprising a plurality of data communications switches, said host computer system and the attached devices each forming a node in a data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture;

including a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture; and

by descriptor logic, generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

It is apparent that Osborne does not teach and does not anticipate a method including a step of "forming said first processing system to comprise a plurality of host computer systems, said second data processing to comprise a plurality of attached devices interconnected by an intervening network architecture, said network architecture comprising a plurality of data communications switches, said host computer system and the attached devices each forming a node in a data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture." Osborne does not

teach and does not anticipate a method including a step of including a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture." Thus claim 10 and all claims that depend on claim 10 are allowable over the cited art

15. As for claims 11-21, Osborne et al teach the claimed limitations as discussed above.

In response, the applicants respectfully state that claims 11-14 are amended to clearly be novel over Osbourne. Claims 11 -14 as amended [with emphasis shown] now read:

11. A method as claimed in claim 10, further comprising,

implementing the network adapter to comprise a pluggable option card having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system, said option card carrying:

an Integrated System on a Chip connected to the bus architecture via a connector,

at least one third level memory modules connected to the chip, and

an interposer connected to the chip for communicating data between media of the network architecture and the chip, said interposer providing a physical connection to the network, and advantageously reducing manufacturing costs and providing reusable system building blocks,
and,

by the descriptor logic, generating a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory.

12. (Currently amended) A method as claimed in ~~claim 10~~ claim 11, further comprising:

implementing the memory by a combination of SRAM and SDRAM, said chip including a memory subsystem of the adapter comprises a first and a second memory, a data cache and an instruction cache associated with a TX processor, and a second data cache and second instruction cache associated with an RX processor, said three levels of memory having respective sizes and associated access times, such that the memory subsystem facilitates: convenient access to instruction and data by both the TX processor and the RX processor; scaleability; and sharing of resources between the TX processor and the RX processor in the interests of reducing manufacturing costs, and

storing the descriptor table in the memory of the first data processing system.

13. A method as claimed in claim 12, further comprising permitting coexistence of heterogeneous communication protocols between adapters and the host system serving various applications, such that use the adapter and a predefined set of data structures enhancing data transfers between the host and the adapter;

opening a number of application channels in parallel as determined by an amount of memory resources allocated to the adapter and being independent of processing power embedded in the adapter. It will be appreciated from the following that the ISOC 120 concept of integrating multiple components into a single integrated circuit chip component advantageously minimizes manufacturing costs and in provides reusable system building blocks. However, it will also be appreciated that in other embodiments of the present invention, the elements of the ISOC 120 may be implemented by discrete components, and

storing the descriptor table in a memory of the second data processing system.

14. A method as claimed in claim 10, comprising forming the descriptor table by linking a plurality of descriptor lists in series via branch descriptors therein, wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors.

using information in the descriptors for control by software in the host of data movement operations performed by TX and RX LCP engines,

using the information to process a frame to generate a TX packet header in the header of the frame.

It is apparent that Osborne does not teach and does not anticipate a method as in claims 11-14. Thus claims 11-14 are each allowable for itself and because it depends on an allowable claim.

Claims 15-21 are each allowable at least because each depends on an allowable claim.

It is anticipated that this amendment brings claim 1-21 to allowance. If any question remains, please contact the undersigned.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

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